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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,320	09/29/2003	Robert M. Ellis	42P17514	4655

8791 7590 03/01/2007  
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EXAMINER
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SCHNEIDER, JOSHUA D

ART UNIT	PAPER NUMBER
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2182

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/674,320	<b>Applicant(s)</b> ELLIS ET AL.	
	<b>Examiner</b> Joshua D. Schneider	<b>Art Unit</b> 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 14 December 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 27-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 27-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.
2. Applicant's arguments filed 12/14/2006 have been fully considered but they are not persuasive. Applicant argues that there is no reason to combine the references. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the rejections clearly state that it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies. Applicant has not addressed the given suggestion to combine the references, and therefore the arguments can not possibly overcome the rejection, as they are not responsive to the rejection.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.

Patent 6,349,390 to Dell et al.

5. With regards to claim 1, Dell teaches a memory system (Fig. 1, element 6) comprising: a memory device (Fig. 1, element 10), a memory controller (Fig. 1, element 28), and a first memory bus to couple the memory device to the memory controller (Fig. 1, elements 14 and 16), wherein, the memory device further comprises: a storage array comprised of a plurality of memory cells (Fig. 1, elements 12a-i); an interface buffer coupled to the storage array (Fig. 1, element 38), and having a first interface to couple the memory device to the first memory bus (column 3, lines 8-22); and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array during a period of time in which there are no transactions carried out by the memory controller on the first memory bus that involve the storage array (column 2, lines 8-35, and column 3, lines 23-64) and, wherein the memory controller accesses the memory device in response to a command issued from any devices and controls functions carried out by the memory device (column 3, lines 18-22).

6. With regards to claim 2, Dell teaches the memory error logic is a component of the interface buffer (column 3, lines 42-47), and wherein the memory device is comprised of a circuit board to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer (Fig. 1, element 10, column 3, lines 8-17).

7. With regards to claim 11, Walker teaches bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the external memory controller and the first interface (column 3, lines 23-64).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,349,390 to Dell et al. in further view of U.S. Patent Application Publication 2002/0167791 to Goris.

10. With regards to claim 3, Dell teaches does not teach the interface has a second point-to-point connection. Goris teaches the interface buffer has a second interface to couple the memory device to a second memory bus to provide a connection between the memory device and another memory device, and the interface buffer passes through bus activity between the first and second memory busses that does not involve the storage array (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Dell using the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

11. With regards to claim 4, Dell does not teach the use of packets, but official notice is given that the use of packets in memory transfers is notoriously well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the

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error correction system of Dell using the notoriously well known use of packets in order to allow the network to transmit longer messages more efficiently and reliably.

12. With regards to claim 5, Dell teaches the memory error logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the storage array (column 6, lines 6-17), providing an opportunity for the memory error logic to proactively carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command from the external memory controller involving the storage array (column 6, lines 17-40).

13. With regards to claim 6, Walker teaches the memory error logic proactively carries out a check for a memory error during a period of time in which a transaction between the external memory controller and the other memory device occurs (column 2, lines 8-35, and column 3, lines 23-64).

14. With regards to claim 7, Dell teaches the memory error logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller (column 6, lines 6-17) by means of a programmable control register (programmed DSP controlled operation, column 6, lines 17-40), providing an opportunity for the memory error logic to proactively carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command involving the storage array (column 6, lines 17-40).

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15. With regards to claim 9, Dell teaches the memory error logic carries out a check for a memory error during an access operation commanded by the external memory controller to determine if there is an indication of a memory error in bits of data being read from the storage array (column 6, lines 17-22).

16. With regards to claim 10, Dell teaches the memory error logic corrects a memory error, if a memory error is detected and is correctable, and the memory error logic transmits a signal to the memory controller if a memory error is detected and is not correctable (column 5, lines 24-58, and column 6, line 22-40).

17. With regards to claim 12, Dell does not teach the use of CRC, but official notice is given that it is notoriously well known in the art at the time of invention to examine CRC information and bus error logic examining the data and the CRC information to check for an occurrence of a bus error. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the well known CRC checking to implement the error correction system of Dell in order to take advantage of the CRC's abilities detecting common errors caused by noise in transmission channels.

18. With regards to claim 8, Dell teaches the memory error logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the memory error logic to opportunistically carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command involving the storage array (powering removed by opening FETs, column 4, lines 1-65).

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19. Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,845,472 to Walker et al. in further view of U.S. Patent Application Publication 2002/0167791 to Goris.

20. With regards to claim 27, Walker teaches a processor (column 3, lines 25-35), a disk storage device coupled to the processor a memory controller coupled to the processor (column 3, lines 36-57), a first memory bus coupled to the memory controller (column 3, line 63, through column 4, line 11), a first memory device having a first storage array comprised of a plurality of memory cells and a first interface buffer coupled within the first memory device to the first storage array (column 4, lines 27-45), and first and second memory error logics associated with the interface buffer to carry out a check for memory errors within the storage array during a period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array (column 8, lines 46-51), but does not teach the interfaces using a point-to-point topology. Goris teaches the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a second interface, a second memory bus coupled to the second interface; and a second memory device having a second storage array comprised of a plurality of memory cells and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the third interface and the second interface, (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using



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the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

21. With regards to claim 28, Walker teaches the memory error logic proactively carries out a check for a memory error during a period of time in which a transaction between the external memory controller and the other memory device occurs (column 5, lines 66, through column 6, lines 29).

22. With regards to claims 29 and 30, Walker teaches the memory error logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller (column 8, lines 46-51, and column 10, lines 8-40) by means of a programmable control register (column 10, line 41, through column 11, line 6), providing an opportunity for the memory error logic to proactively carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command involving the storage array (column 10, lines 8-40).

23. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,845,472 to Walker et al. and U.S. Patent Application Publication 2002/0167791 to Goris in further view of U.S. Patent 6,349,390 to Dell et al.

24. With regards to claim 31, Walker and Goris fail to teach the powering down of the inactive bus, but Dell teaches the memory error logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the memory error logic to opportunistically carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory

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error without delaying the carrying out of an access command involving the storage array (powering removed by opening FETs, column 4, lines 1-65). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the power removed error checking of Dell with the combined error correction system of Walker and Goris in order to correct memory errors quickly and without interruption.

### ***Conclusion***

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M-F, 8-4:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDS



**KIM HUYNH**  
**SUPERVISORY PATENT EXAMINER**  
2/27/08